JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **5** No 2, 02009(3pp) (2013)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **5** № 2, 02009(3cc) (2013)

Surface Passivation of Germanium Using NH_3 Ambient in RTP for High Mobility MOS Structure

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(Received 15 February 2013; revised manuscript received 30 April 2013; published online 04 May 2013)

Ge CMOS is very striking for the post Si-CMOS technology. However, we have to attempt a number of challenges with regard to materials and their interface control. In this paper we have investigated the control of the interfacial properties of SiO_2 / Ge gate stack structures by the thermal nitridation technique. Structural and electrical properties of SiO_2 gate-dielectric metal-oxide-semiconductor (MOS) capacitors deposited by sputtering on germanium are studied. The structural characterization confirmed that the thin film was free of physical defects and smooth surface of the films after PDA at 500 °C in N_2 ambient. The smooth surface SiO_2 thin films were used for Pt / SiO_2 / GeON / Ge MOS structures fabrication. The MOS structure yields a low leakage current density of 9.16×10^{-6}A·cm^{-2} at 1 V.

Keywords: Germanium, Passivation, SiO_2, RF-Sputtering, Leakage current

PACS numbers: 77.55. + f, 81.20.Fw, 68.37, Hk, 85.30.Tv, 84.37. + q

1. INTRODUCTION

As the constant scaling of Si metal-oxide-semiconductor (MOS) devices approaching its primary limits, a variety of modified channel materials, such as a strained Si, are being considered to increase the drain current by improving the carrier mobility in the channel region. An alternative approach is to continue the trend of scaling by implementing novel channel materials with better transport properties than silicon. Among the studied materials the carbon nanotubes, silicon nanowires, graphene, Ge and III-V compound semiconductors such as InSb and InGaAs which have significantly higher intrinsic (*p* or *n*) mobility than silicon[1-4]. Germanium is being considered as a potential channel material for the next generation MOS devices due to its much higher low field electron (two times higher) and hole (four times higher) mobilities than Si [5-6]. One of the serious issues in establishing Ge-based CMOS technology has been the effective passivation of Ge surfaces by dielectrics with better interface properties [7-8]. The establishment of fabrication technology for high-performance Ge gate stack structures is required for future Ge MOS devices. Different passivation techniques have been employed to form the stable surface over the Ge to get the superior interface properties such as nitridation, sulfur passivation, Si passivation etc [9-10]. In this work we have performed the thermal nitridation of Ge in NH_3 ambient using RTP system for the passivation of germanium surface [11]. Since SiO_2 has proven to be best insulator for the success of Si semiconductor technology since last few decades [12]. SiO_2 has high band gap (9 eV), high dielectric strength of 10^7 V/cm, compatibility with polysilicon gate process, excellent thermal stability with silicon, low density of interface states and good electrical reliability [13]. In this work the deposited SiO_2 is used as gate dielectric over the surface passivated germanium for the fabrication of Ge / GeON / SiO_2 gate stack. RF sputtering is physical vapor deposition (PVD) based technique combined with plasma offers a low temperature processing and blocks the oxygen from the ambience, which prevents the formation of interfacial layer (IL). Hence, good quality of gate dielectric thin films can be achieved using RF-Sputtering technique which is important in the fabrication of CMOS devices [14].

In this study, the surface properties of SiO_2 films on Ge substrates with special attention on the leakage current in MOS capacitors is investigated after Ge passivation using rapid thermal nitridation in NH_3. Second section of the paper describes the experimental details, third section includes the results and discussion part and fourth section concludes the paper.

2. EXPERIMENTAL DETAILS

Germanium substrates with resistivity of 0.01-0.1 Ω·cm were used for deposition of SiO_2 thin films. The 2" *p*-type Ge (100) substrates were cleaned using cyclic HF DI rinse. The substrates were rinsed in 2 % HF and de-ionized water alternately for several times, followed by blowing dry with N_2. Following that, annealing in a NH_3 ambient was performed inside a RTP chamber at a constant temperature of 550 °C for four minutes. Substrates were then transferred to the sputtering chamber for the deposition of SiO_2 thin films. The process parameters like base pressure, operating pressure, sputtering distance, sputtering time for the deposition of SiO_2 were set as 4.0×10^{-5} mbar, 0.022 mbar, 13.5 cm and 11 minute respectively at room temperature using the Argon plasma. Post deposition annealing (PDA) was performed in N_2 ambient at 500 °C for 60 s under atmospheric pressure using rapid thermal annealing. To study the leakage current behavior Platinum metal was deposited as top electrode on SiO_2 thin films through shadow mask with electrode area of 12.56×10^{-4}cm^2 by using metal sputtering system (Nordiko) at base pressure of 2.3×10^{-5} mbar where substrate was kept at room temperature. The

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native oxide was removed by the Buffered Hydrofluoric Acid (BHF) followed by rinsed in deionized water before the back contact formation. An ohmic contact was formed on backside of Ge substrate to form MOS capacitors by thermally evaporating the Al metal. These fabricated Pt / SiO_2 / GeON / Ge MOS capacitors were post metallization annealed (PMA) at 450 °C for 20 min using forming gas (90 % N_2, 10 % H_2) ambient. The structural characterization of annealed SiO_2 films was carried out by using the ellipsometer (Philips SD 1000), XRD (BRUKER Model D8 ADVANCE) and AFM. Current as function of voltage, I-V (semiconductor characterization system 4200) measurements of fabricated MOS structures were performed to study the electrical properties.

3. RESULTS AND DISCUSSION

3.1 SEM / AFM

Fig. 1 shows the typical surface morphology of SiO_2 thin film annealed at 500 °C examined by SEM. It is observed that samples do not reveal any physical defects such as cracks and void under the investigated magnification from low (20 k×) to high (75 k×). Two and three dimensional (2 and 3D) surface topographies

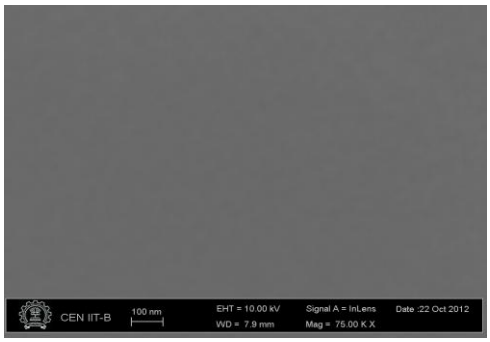

Fig. 1 – A typical SEM micrograph of SiO_2 film deposited on surface passivated Ge and PDA at 500 °C

of the investigated SiO_2 thin film were examined using AFM with a scanning area of 1 × 1 μm shown in Fig. 2a and b. The topography of the sample annealed at a 500 °C temperature was smooth and the root-mean-square (RMS) surface roughness for the deposited films was found to be 2.15 nm. 2D image showed the uniform, homogeneous distribution of the grains over entire film. 3D image revealed pyramid like nanostructure with almost uniform height.

3.2 Ellipsometer

The thickness and refractive index (RI) measurement was done using Philips SD 1000 ellipsometer in raster scan method at 16 different points on the film surface at wavelength of 632.8 nm. Thickness of the GeON / SiO_2 bilayer dielectric stack was measured to be in the range of 27.69-28.57 nm. The thickness of interfacial GeON layer was approximately 5.52-5.79 nm. The refractive index value for dielectric stack was found to be in the range of 1.46-1.49. The measured RI value of dielectric stack is close to the RI value of SiO_2. The thickness and RI topographies are shown in Fig. 3a and b respectively, the measurement

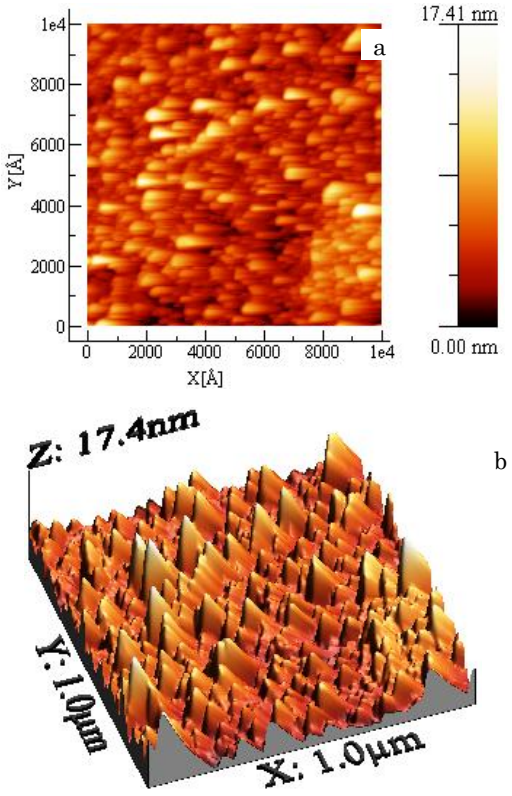

Fig. 2 – Two-dimensional AFM topography of SiO_2 film deposited on surface passivated Ge and PDA at 500 °C (a). Three-dimensional AFM topography of SiO_2 film deposited on surface passivated Ge and PDA at 500 °C (b)

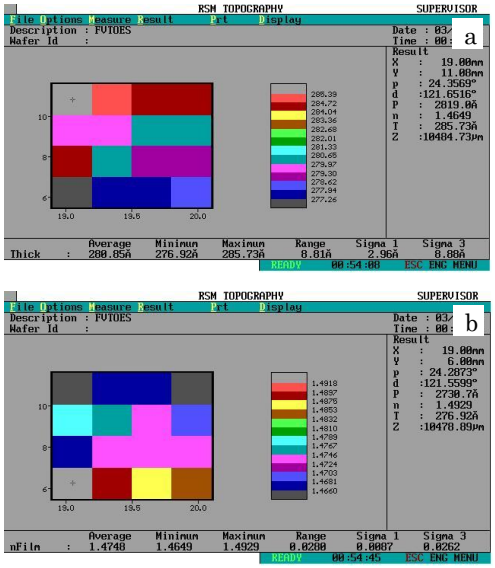

Fig. 3 – Thickness topography of SiO_2 film deposited on surface passivated Ge and PDA at 500 °C (a). Refractive index topography of SiO_2 film deposited on surface passivated Ge and PDA at 500 °C (b)

shows good uniformity of the film with excellent coverage as confirmed through AFM and SEM results.

3.3 XRD

XRD measurement of SiO_2 films after annealing at 500 °C temperature was carried out to examine the crys-

tal structure of SiO_2 films deposited on germanium. It was found that there was tetragonal (*t*) phase in our SiO_2 films with two orientations of the SiO_2 thin film at (6 5 2), (12 2 1) planes were observed. The diffraction planes are well matched with ICDD file number 00-089-1688, which is associated with the SiO_2 phase as shown in Fig. 4. In the XRD spectra the dominant peak observed at 37.55° (2θ) corresponds to the germanium substrate. Besides that, two additional peaks identified as germanium oxide nitride with an ICDD file number of 00-026-0685 oriented at (2 2 3) (5 1 3) is detected along with the aforementioned three peaks corresponding to nitride interfacial layer.

3.4 Current-Voltage Measurement

Leakage current behavior of the fabricated MOS structure is verified using the I-V measurement. The leakage current density characteristics of the investigated samples post metallization annealed (PMA) at 450 °C temperature is shown in Fig. 5. The leakage current density of devices with 500 °C annealed SiO_2 film is 9.16×10^{-6} A·cm^{-2} at 1.0 V, which is slightly lower than the leakage current density, previously reported by Xue-Fei Li et al for HfO_2 / SiO_2 gate stack on Ge substrates [15] and by us for HfO_2 grown by RF sputtering technique on silicon substrates [16].

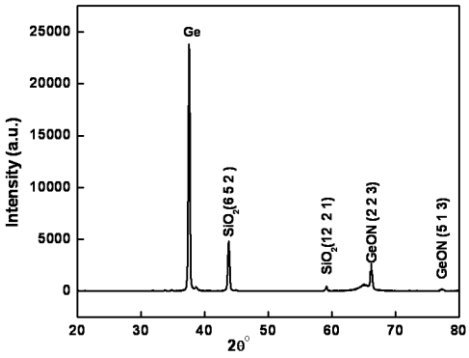

Fig. 4 – XRD spectra of SiO_2 film deposited on surface passivated Ge and PDA at 500 °C

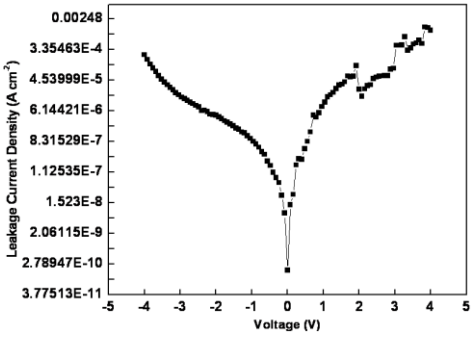

Fig. 5 – J-V characteristics of Pt / SiO_2 / GeON / Ge MOS capacitor PMA at 450 °C

4. CONCLUSIONS

In summary, the Ge surface has been effectively passivated by NH_3 annealing in RTP system. The physical and electrical properties of RF sputtered SiO_2 / Ge MOS capacitors have been investigated. It is found that GeON is formed during surface nitridation (NH_3 annealing) of germanium. SiO_2 films deposited on nitrided germanium are observed to be smooth surfaced and crack free. Ellipsometer and AFM confirmed the uniformity of the film. In addition, the electrical characteristics of SiO_2 Ge MOS capacitors showed that surface nitridation is very effective to improve the leakage current density. This concludes that the fabricated MOS structures can be useful for high mobility devices due to high mobility of carriers in germanium.

ACKNOWLEDGMENT

Authors are thankful to CEN, IITB for providing necessary fabrication and characterization facilities under INUP scheme. One of the author A. G. Khairnar is thankful to CSIR New Delhi, India for providing senior research fellowship for carrying out this work (vide File No. 09/728(0029)/2012-EMR-I).

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